Analysis on DC link filtering capacitor stress of an inverter for embedded systems

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***Abstract*—This paper deals with the modeling of a 3-phase-2-level inverter in an embedded environment (in which the power source is a battery) with a focus on the dimensioning aspect of capacitors used for filtering the voltage ripple at the input of the inverter. Indeed, these capacitors must, firstly, ensure an acceptable voltage ripple level (defined by users) and, secondly, be able to support the rms current flowing through them (defined by capacitor manufacturers). These two constraints are analyzed using SVPWM (Space Vector Pulsewidth Modulation) strategy at different switching frequencies. The aim of this paper is to show that "second order" phenomena (ESR, printed track resistance, temperature) have to be taken into account for an optimal sizing of the DC link capacitors.**

***Index Terms*—Inverter, embedded applications, DC link, modeling, PWM strategy, chemical capacitor**

I. Introduction

More and more electronic equipments are used in automobile. The research for reliable and compact electronic equipments is crucial due to their increasing density in a very limited volume (an automobile). Dimensioning of power electronics converters, particularly filtering capacitors located at the input of voltage source inverters (VSI), is a part of these researches. The objective of this study is to evaluate the current stress in chemical capacitors, with a totally characterized test bench representing the power supply system for an electric motor (starter-generator) in an automobile, and to evaluate the DC link voltage ripple level according to the chosen values of these capacitors. In fact, the choice of the capacitor value can be conditioned by the current flowing through them (and this current can not exceed a maximum value given by the manufacturer) or by the DC link voltage ripple level for a given operating condition (a defined load with a given power factor).

First, the whole test bench and the retained model for each of its elements is presented. In particular, the model of electrolytic capacitors ($R-C$ series model) will be detailed, the analytical relation of these two parameters is established based on technical documentation of a manufacturer. Finally, the system is simulated and tested in real situation with a reference modulation strategy (Space Vector PWM); the results will be analyzed.

II. Presentation and modeling of the test bench

A. Global presentation of the system

The results in this paper are based on a test bench representing a embedded low voltage application (e.g. automobile). The parameters of this system are identified either by experiment [1] (for polypropylene capacitor, cable, load) or by manufacturer data (electrolytic capacitor, MOSFET, battery).

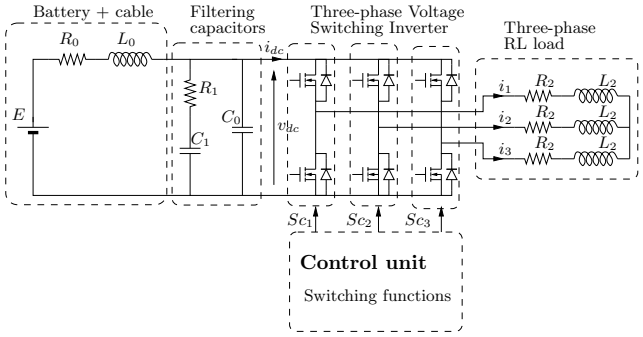

Figure 1. The inverter model and its environment

- A lead-acid battery with an internal resistance of $10m\Omega$.
- 1.5m long DC link cable with the self-inductance of 1.5 μH and the resistance of $4m\Omega$. In the lump circuit model shown in fig. 1, this resistance is coupled with the battery's resistance to give a total resistance of $14m\Omega$.
- Electrolytic capacitors at the input of the inverter are modeled using $R-C$ series model (this model will be detailed in the next part of this paper).
- 6 polypropylene capacitors of 10µF each, these capacitors are considered ideal for the frequency range in which we are interested (<1MHz).
- 3 phase 2 level inverter made up of 6 MOSFETs (caliber 100V/500A) with an on-state resistance of $R_{DSon} = 3m\Omega$. The PWM strategy used for this study is Space Vector PWM (SVPWM).
- 3 phase inductive load $R-L$ with the phase inductance of 408µH and the phase resistance of $52m\Omega$.

Fig. 1 shows the global model of the system.

B. Electrolytic capacitor modeling

In this study, electrolytic capacitors are modeled using RC series circuit, where the capacitance is noted C_1 and the resistance is noted R_1. Using the technical documentation of different manufacturers, the following formula is proposed by the authors to model the relationship between these two quantities:

$$R_1[m\Omega] = r_0[m\Omega] + \frac{\tau_0[ns]}{C_1[\mu F]} \quad (1)$$

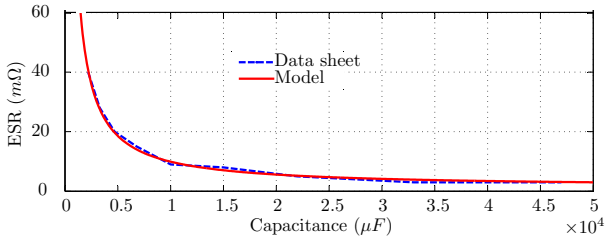

Figure 2. Comparison of model and Datasheet on Equivalent Series Resistance (ESR) according to the capacitance value

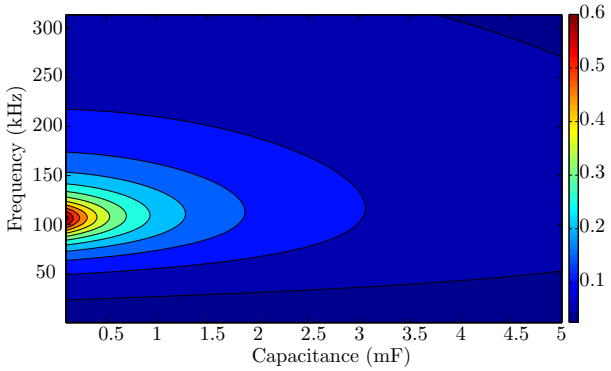

Figure 3. DC link bus's impedance amplitude in function of frequency and electrolytic capacitor value (with its associated equivalent series resistance)

Likewise, the proposed formula to model the relationship of the RMS current I_{AC} supported by the capacitors, given by manufacturers, and their capacitance is:

$$I_{AC}[A] = I_0[A] + k.C_1[\mu F] \tag{2}$$

For EVOX RIFA PEG 225-25VDC capacitors [2], $r_0 = 3.6m\Omega$, $\tau_0 = 18250ns$, $I_0 = 10.56A$ and $k = 2.93.10^{-3}A/\mu F$.

Figure 2 presents a comparison between the model with equation 1 and datasheet of the value of R_1 according to the value of C_1. There is a good concordance between these two curves.

An observation can be drawn from equation 2 that it is more interesting to associate capacitors with small capacitance value than to use only one capacitor with a big value. Indeed, the current caliber of the association of small capacitors is greater than the current caliber of one capacitor with an equivalent capacitance. Similarly, the equivalent value of the resistance can be reduced by an association (in parallel) of capacitors, however, the gain in reality is moderated due to very small value of the asymptotic resistance r_0 in equation 1.

This model is named as model 1 for the rest of the article.

C. Simulation tool

The simulation tool used in this article is developed under Java with a simple "fixed step Euler" solver. The advantage of this simulation tool is that it allows users to have a large degree of modularity when associating physical objects represented by informatic objects (Object Oriented Programming). Il also requires less calculating time in comparison with Matlab/Simulink thanks to a lighter programme; this is particularly important for parametric studies presented in the next section which could have required many computer ressources and long calculating time in order to get the results for different values of electrolytic capacitors if using Matlab/Simulink. Finally, the chosen time step of $10^{-8}s$ allows us to have a stable and precise simulation with a reasonable computation time.

III. Parametric study of the system

A. Dc link bus impedance:

The impedance of the DC link bus (seen from the inverter) is:

$$Z_{bus} = \frac{V_{dc}}{I_{dc}} = \frac{(R_s + jL_s\omega)(\frac{1+jR_1C_1\omega\frac{1}{jC_0\omega}}{j(C_0+C_1)\omega - R_1C_1C_0\omega^2})}{(R_s + jL_s\omega) + (\frac{1+jR_1C_1\omega\frac{1}{jC_0\omega}}{j(C_0+C_1)\omega - R_1C_1C_0\omega^2})} \tag{3}$$

where R_s, L_s, and C_0 are known and fixed parameters, and R_1 and C_1 are variable parameters and are coupled with the formula 1. V_{dc} and I_{dc} are the voltage and the current at the DC terminals of the inverter.

The electric energy is fed to the load by the switching process of the inverter, and this process will induce "jumps" of the instantaneous value of the current I_{dc}. If the value of Z_{bus} is strong then the value of V_{dc} fluctuates greatly. Therefore, in order to limit the fluctuation of V_{dc}, the value of Z_{bus} must be small. The voltage V_{dc} can also fluctuate greatly when a harmonic component of current I_{dc} situates in the resonance zone of Z_{bus}.

Fig. 3 shows that for capacitance values under 3mF, a resonance zone is visible. For capacitors with greater capacitance, the magnitude of the impedance is almost constant in the low frequency range. A modest increase of the magnitude can be constated in the frequency zone ranging from tens of kilohertz to hundreds of kilohertz. This is the zone where most of the I_{dc} current spectrum component is located.

B. Simulation results

The system is simulated in time domain in order to evaluate the DC link voltage ripple and the RMS current flowing through electrolytic capacitors.

Hereby, we present the synthetically results of simulation in terms of DC link voltage ripple ratio (fig. 5) and the ratio between the observed RMS current value/ maximal RMS current supported by the capacitors (fig. 4). In these two results, the variable parameters are the switching frequency and C_c value (and its associated equivalent series resistance).

These results allow us to define operating points (with the same PWM strategy) where the criteria are met or not (tab.I). The chosen criteria are

- DC link voltage ripple level inferior to 10% of the constant DC link voltage value.

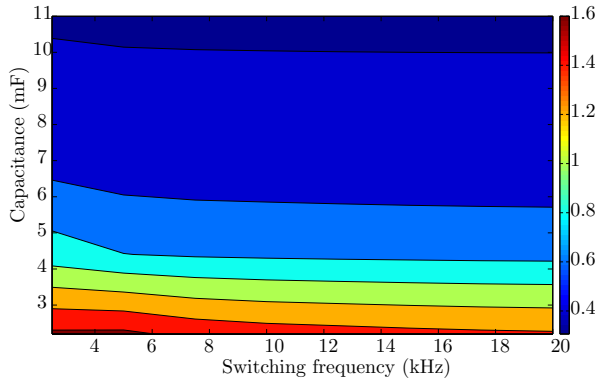

Figure 4. RMS current/I_{AC} in function of switching frequency and the value of C_c (and the associated ESR value)

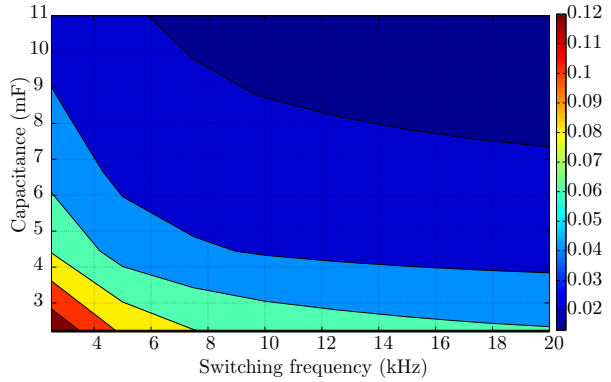

Figure 5. Dc link voltage ripple ratio in function of switching frequency and value of C_c (and the associated ESR value)

- The ratio between the observed RMS current value in electrolytic capacitors/maximal RMS current value supported inferior to 1.

The box where the value is 2 indicates that the voltage ripple level is too high and the RMS current in the capacitors is too high as well according to chosen criteria. The boxes where the values are "1" indicates that only one criterion is not satisfied. In this table, the boxes contain the value 1 means that the RMS current in the electrolytic capacitors is greater than their supported values. The boxes where the value is "0" mean that these operating points satisfy the two criteria.

From these the figures and the table, we can conclude that for the defined criteria (DC link voltage ripple under 10% and the capacitor current smaller than the supported value), with SVPWM (Space Vector PWM) and with this capacitance step, capacitors (or set of capacitors) of at least 4400μF are

		Switching frequency (kHz)							
		2.5	5	7.5	10	12.5	15	17.5	20
$C_c[\mu F]$	2200	2	1	1	1	1	1	1	1
	4400	0	0	0	0	0	0	0	0
	6600	0	0	0	0	0	0	0	0
	8800	0	0	0	0	0	0	0	0

Table I
TABLE OF NON-SATISFACTION OF THE CRITERIA FOR EACH OPERATING POINT

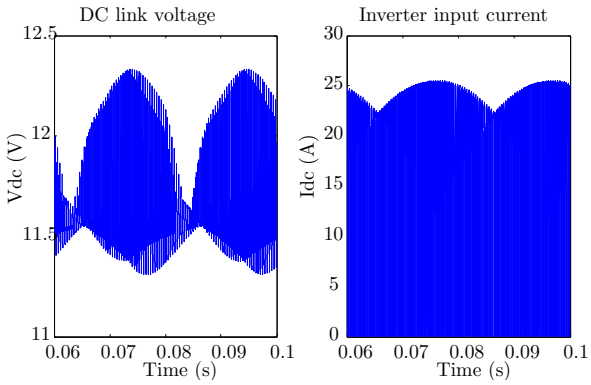

Figure 6. DC link voltage and inverter input current for the case of $C_c = 2200\mu F$ and switching frequency at 2.5kHz

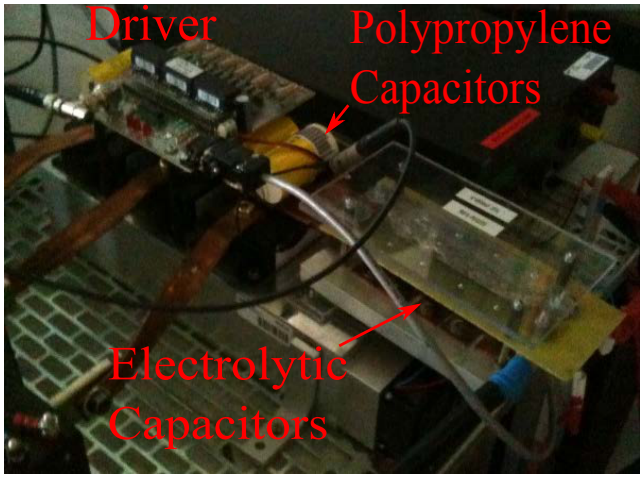

Figure 7. Test bench

suitable. When using capacitor of 2200 μF, with the switching frequency at 2.5 kHz, none of the two criteria is met (RMS current and DC link voltage ripple are too high see figure 6). Of course, capacitor value step can be finer in order to achieve the optimal solution.

IV. Experiment results

A. Test bench description

The test bench includes the elements presented in the introduction (see fig. 7). Figure 8 illustrates a set of 4 electrolytic capacitors put in parallel and mounted on a thermal dissipator. A copper sheet is used to cover each capacitor in order to drain the heat to the aluminum dissipator. The switching commands for the three half-bridges are carried out with help of the DSP board Taxas Instruments TMS320F2812. The Space Vector PWM strategy is implemented, with the switching frequency of 10kHz.

B. Thermal surveillance

The tests are carried out with high load current. A thermal camera is used to observe the temperature evolution of electrolytic capacitors. It can be observed that the temperature on these capacitors stays in the range of 40°C to 45°C, which

Figure 8. Electrolytic capacitors mounted on the thermal dissipator

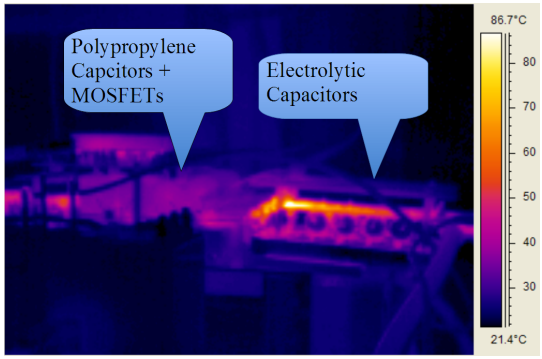

Figure 9. Temperature distribution on the inverter after 30 min of operation

is relatively modest for a device under high stress, after 30 minutes of operation (see fig.9). On the other hand, it can be seen that the hottest point on the whole system is the printed track shown in fig. 8. This $70\mu m$ thick and $35mm$ large printed track is used to connect the 4 electrolytic capacitors and the DC link. It is, therefore, recommended to modify to model in order to take into account the temperature increase phenomenon on printed track and capacitors.

C. Model fitting

Due to high temperature in the printed track, it is necessary to take into account the resistance of this element. A measurement of voltage drop between the input and output of the track (0.112V under 20A DC) allows estimating its equivalent resistance ($5.6m\Omega$). With the assumption that this resistance is divided into several equal resistors, the retained model is presented in fig. 10 with $r_1 = 1.12m\Omega$. Furthermore, as the operating temperature of the capacitors is estimated at 45°C and their equivalent series resistance (ESR) (given in the datasheet) varies from $28m\Omega$ (100kHz at 25°C) and $7.3m\Omega$ (100kHz at 125/150°C) , the retained ESR value is $R_1^{'} = 18m\Omega$. Thus, with 4 capacitors, the total capacitance is $19.2mF$ and the global ESR is $4.5m\Omega$. All other things being equal, the model with the above modifications is called model 2 for the rest of this article.

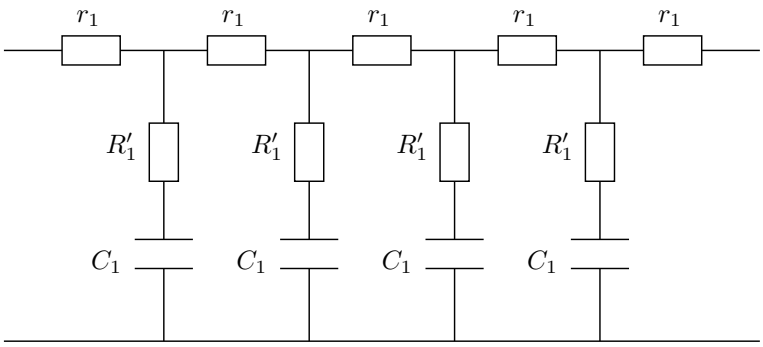

Figure 10. Equivalent electric circuit for electrolytic capacitors and the printed wire

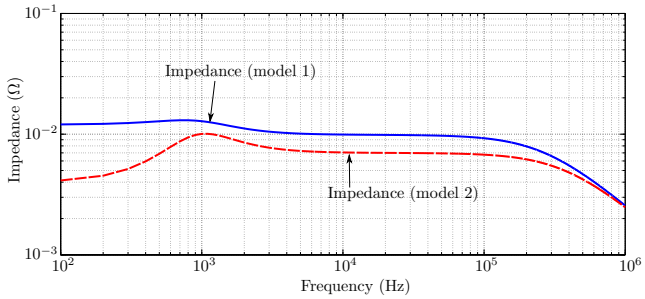

Figure 11. Global impedance of DC link seen by the inverter of model 1 and model 2

The simulation results show that peak to peak ripple value of DC link voltage with model 1 is 0.55V whilst with model 2, this value is 1.1V (the experimental value is 2V). Indeed, the spectrum in figure 11 shows that the global impedance of the DC link seen by the inverter in model 2 is strongly modified in comparison to model 1. This modification allows us to get a voltage ripple level closer to the experimental result.

Figure 12 presents a comparison in frequency domain of the simulation results with model 1, model 2 and experimental results for DC link voltage. In the zone from 100Hz to 10kHz, theorically, this is an "empty" zone, which means that the curve shown in this figure represents noise. The zone in which we are interested is the zone form 10kHz (switching frequency) to 100kHz. In this zone, the disturbances can be considered as generated by the switching effect of the implemented PWM strategy. On the figure, a good concordance between the simulation result (model 2) and experimental result can be observed. Therefore, it can be concluded that this model is suitable to evaluate the impact of different PWM strategies on the DC link voltage ripple.

V. Conclusion

This paper presents a model of an embedded application, this model is validated by experimental results and is used for filtering electrolytic capacitor "optimal dimensioning". The difficulty to model such a system, embedded low voltage/ high current inverter, in terms of the system sensibility related to connectic was also demonstrated. Time and frequency analysis allows evaluating quickly the impact of PWM strategy on the DC link voltage quality and on the respect of capacitor

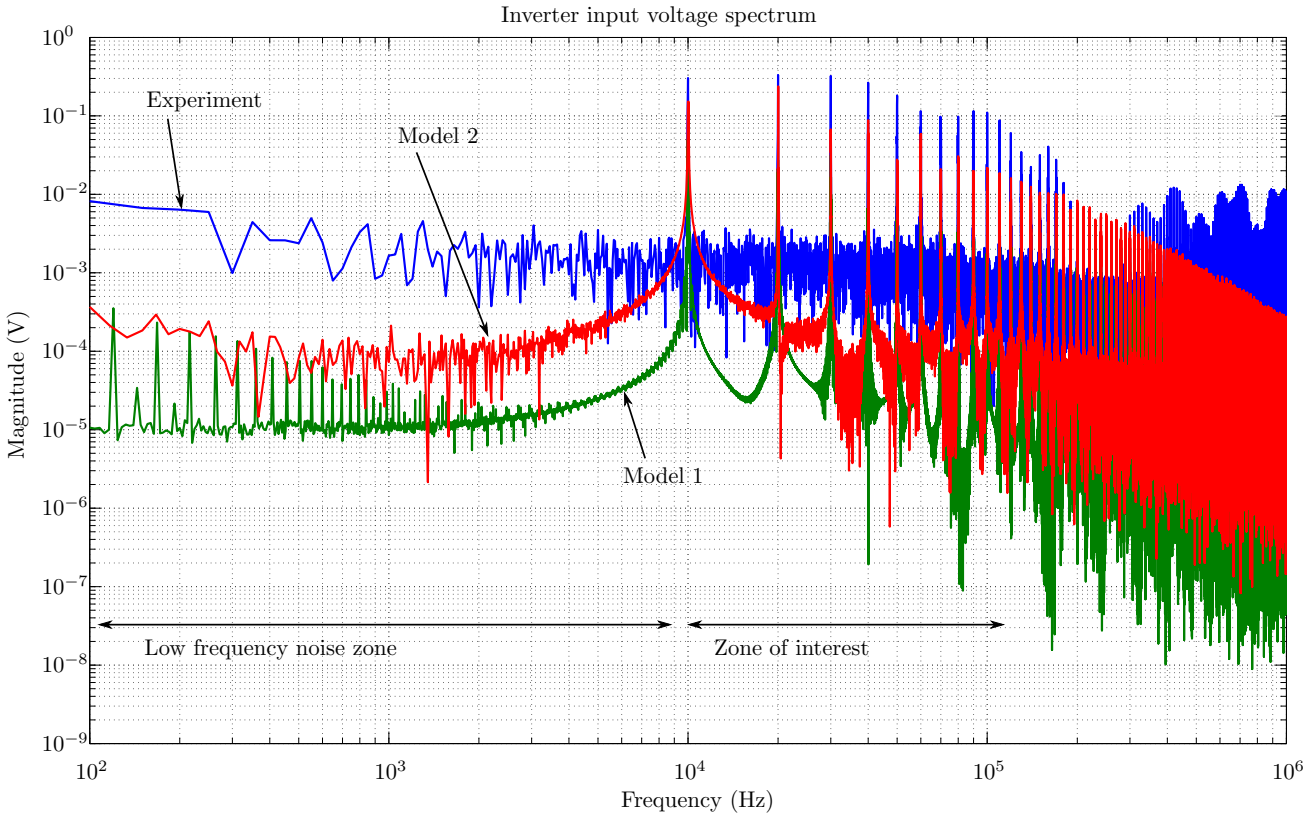

Figure 12. DC link voltage ripple spectrum (experiment/model 1/ model 2)

stress constraints. These models will be used to evaluate the influence of PWM strategies prensented in [3], [4] on the DC link capacitor current and DC link voltage ripple level.

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